Ch-5 - Pipelining And Vector Processing.

1 Explain Pipeline with 4-Segment.

=) Pipelining is a technique of decomposing a sequential process into sub-operation.

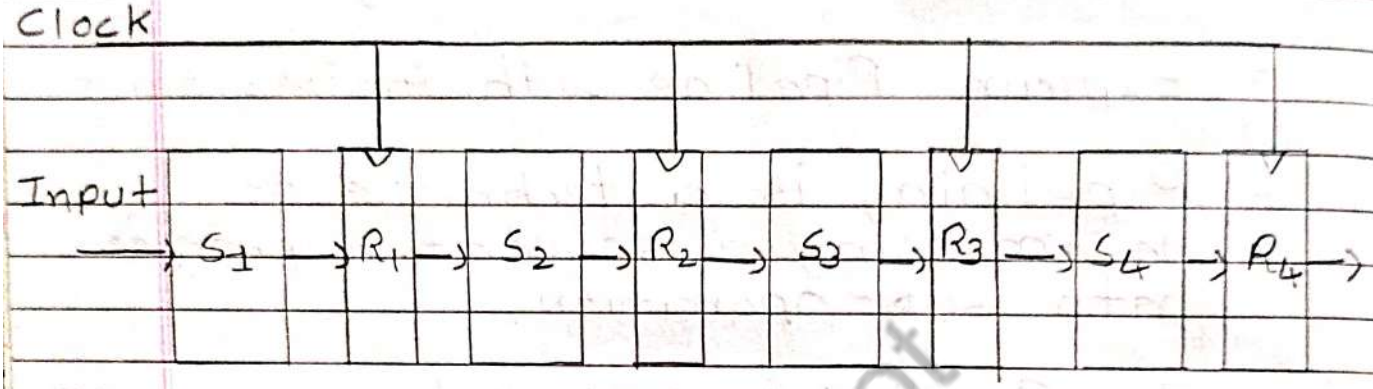
In Pipelining each sub-operation being excuted in a dedicated segment.

Every sub operation have different segment to perform the operation.

The structure of a pipeline can be represented by including an input register for each segment followed by a combinational circuit.

For 4-Segment Structure, we require 4 input register and 4-Segment.

For n-segment structure, we require n input register and n-segment.



Here, R_1, R_2, R_3 and R_4 are input Register and S_1, S_2, S_3 and S_4 and segment.

All the input Register are connected with same clock.

Spce-Time Diagram:

Segment \ t	1	2	3	4	5	6	7	8	9
1	T_1	T_2	T_3	T_4	T_5	T_6			
2		T_1	T_2	T_3	T_4	T_5	T_6		
3			T_1	T_2	T_3	T_4	T_5	T_6	
4				T_1	T_2	T_3	T_4	T_5	T_6

→ Clock cycle

2. Explain Floating Arithmetic Pipeline with example.

=> Floating Arithmetic Pipelines are mostly used in high-speed computers.

Floating Arithmetic Pipelines are used to implement floating point operation.

There are 4-Segment to Perform Floating Arithmetic pipelines.

1) Compare the Exponents
2) Align the mantissas
3) Add or Subtract the mantissas
4) Normalize the result

Ex. $X = 0.9504 * 10^3$

$Y = 0.8200 * 10^2$

1 Compare the Exponents:

In this example, 2 and 3 are exponents.

The large exponent is chosen as the exponent of the resut.

We have to compare exponents and perform subtraction operation.

The difference of exponents =

$\therefore 3 - 2 = 1$

2 Align the Mantissas:

After the Finding the difference of exponents, we have to shift mantissas according to difference of exponents.

Here, Difference of Exponents = 1

$X = 0.9504 \times 10^3$

$Y = 0.08200 \times 10^3$

3 Add or Subtract Mantissas:

After that, we have to Perform addition or subtraction Operation on Mantissas.

Here, We Perform addition operation,

$X + Y = 1.0324 * 10^3$

4 Normalize the result

Here, Value of X and Y are form of 0. value. So, Answer of X and Y should be form of 0. value.

So, $Z = X + Y = 0.10324 \times 10^4$

3 Explain 4- Stage Instruction Pipeline.

=> In Digital Computer, Complex instruction require instruction pipeline to carry out operation like fetch, decode and execute instruction.

The Computer needs to proceess each instruction with the following e sequence of steps.

1) Fetch instruction from memory
2) Decode the instruction
3) Calculate the effective address
4) Fetch the operands from memory
5) Execute the instruction
6) Store the result

Instruction pipeline will be more efficient if the instruction cycle divided into segments of equal duration.

There are 4-Stage or 4-Segment of Pipelinae.

(1) FI : Fetch an instruction From memory

(2) DA : Decode the instruction and calculate effective address.

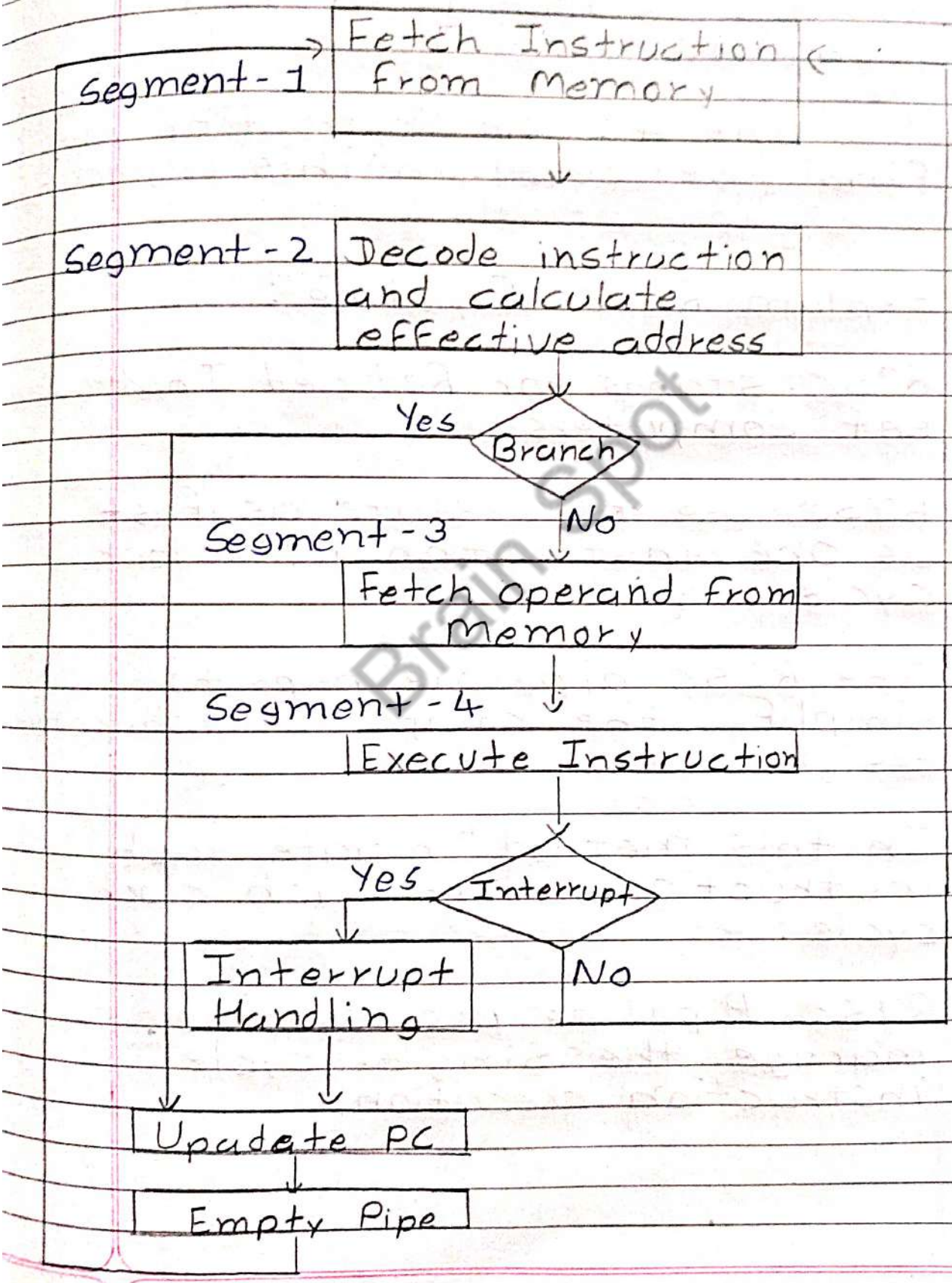
(3) FO : Fetch the Operand

(4) EX : Execute the operation.

4-Segment of Pipeline:

1 Segment-1 : The instruction can fetch segment can be implement using FIFO buffer.

2 Segment-2 : The instruction is decoded and calculate the effective address.


Segment - 1
Fetch Instruction from Memory
Segment - 2
Decode instruction and calculate effective address
Yes
Branch
No
Segment - 3
Fetch Operand from Memory
Segment - 4
Execute Instruction
Yes
Interrupt
No
Interrupt Handling
Update PC
Empty Pipe

3 Segment-3 : An operand from memory is feched in this segment.

4 Segment-4 : The instruction are finally executed in this segment.

4 Explain RISC Pipeline :

RISC stands for Reduced Instructio Set Computers.

RISC use to execute as fast as one instruction per clock cycle.

The RISC pipeline helps to simplify the computer architecture design.

In this method, initiate each instruction with each clock cycle.

RISC Pipeline processor to manage the Single-cycle instruction execution.

RISC compiler gives support to translate the high-level language program into a machine language program.

RISC Processor can follow this three type of instruction.

1 Data Manipulation Instruction:

I : Instruction Fetch
A : Decode, Read Registers
E : Write a Register

2. Load and Store Instruction:

I : Instruction Fetch
A : Decode, Evaluate Effective Address
E : Register to Memory or Memory to Register

3 Program Control ~~St~~ Instruction:

I : Instruction Fetch
A : Decode the Instruction and Evaluate Effective Address.
E : Write Register (PC)

5 Explain RISC Stage:

There are 5 Stage of RISC Processor.

1) Instruction Fetch
2) Instruction Decode
3) Instruction Execute
4) Memory Access
5) Write Back

1 Stage 1: Instruction Fetch:

In this stage, the CPU reads instructions from the address in the memory.

2 Stage 2: Instruction Decode:

In this stage, Instruction is decoded and the register file get values from the register.

3 Stage 3: Instruction Execute:

In this stage, ALU operation are performed.

4 Stage 4: Memory Access:

In this stage, memory operands are read or write from memory or to memory.

5 Write Back: stage 5

In this stage, fetched value is ~~wrri~~ written back to the Register.